

IN THE CLAIMS:

A. Please amend claims 1-5 as follows:

Amended Claims With Mark-ups to Show Changes Made

1. (Amended) A semiconductor device comprising:
a semiconductor substrate having a first conductivity type;
a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
[a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;]
a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well; and
[a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well;]
a heavily doped region of buried layer having the second conductivity type formed between [at a portion corresponding to] the first contact region in the first well and an interface between the first well and the semiconductor substrate; and
a heavily doped region of buried layer having the first conductivity type formed at a portion corresponding to the second contact region in the second well].

2. (Amended) The semiconductor device as claimed in claim 1, [wherein the heavily doped regions of buried layers having the first and second conductivity types are spaced at a distance of about 0.25 to 1.0 μm beneath the major surface of the semiconductor substrate.]
further comprising:

a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;

a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and

a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between the second well and the semiconductor substrate.

3. (Amended) The semiconductor device as claimed in claim 2 [1], wherein the junction depth of the first and second wells is 1.5 to 2.0 μm .

4. (Amended) The semiconductor device as claimed in claim 2 [1], wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

5. (Amended) The semiconductor device as claimed in claim 2 [1], wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

Clean Set of Amended Claims

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1. (Amended) A semiconductor device comprising:
a semiconductor substrate having a first conductivity type;
a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well; and
a heavily doped region of buried layer having the second conductivity type formed between the first contact region in the first well and an interface between the first well and the semiconductor substrate.
 2. (Amended) The semiconductor device as claimed in claim 1, further comprising:
a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;
a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and

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a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between the second well and the semiconductor substrate.

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3. (Amended) The semiconductor device as claimed in claim 2, wherein the junction depth of the first and second wells is 1.5 to 2.0 μm .

4. (Amended) The semiconductor device as claimed in claim 2, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

5. (Amended) The semiconductor device as claimed in claim 2, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

B. Please add new claims 11-25 as follows:

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11. (New) The semiconductor device as claimed in claim 2, wherein the heavily doped region having the first conductivity type does not extend under the second MOS transistor in the second well.

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12. (New) The semiconductor device as claimed in claim 1, wherein the heavily doped region of the second conductivity type does not extend under the first MOS transistor in the first well.

13. (New) The semiconductor device as claimed in claim 1, further comprising: a second well having a first conductivity type formed in a second region of the semiconductor substrate, wherein the heavily doped region of buried layer having a second conductivity type is not formed at an interface between the first and second wells.

14. (New) The semiconductor device as claimed in claim 1, further comprising: a second well having a first conductivity type formed in a second region of the semiconductor substrate; and a heavily doped region of buried layer having a first conductivity type not formed at an interface between the first and second wells.

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15. (New) A semiconductor device, comprising:
a semiconductor substrate;
a first well having a second conductivity type formed in a first region of the
semiconductor substrate;
a second well having a first conductivity type formed in a second region of the
semiconductor substrate; and
a heavily doped region of buried layer having a second conductivity type not
formed at an interface between the first and second wells.

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16. (New) The semiconductor device as claimed in claim 15, wherein the
semiconductor substrate has a first conductivity type and the first and second wells are formed
in a major surface of the semiconductor substrate.

17. (New) The semiconductor device as claimed in claim 15, further comprising:
a heavily doped region of buried layer having a first conductivity type not formed
at an interface between the first and second wells.

18. (New) The semiconductor device as claimed in claim 17, wherein the
concentration of the heavily doped region of buried layer having the first conductivity type is
higher than that of the second well and lower than that of the second contact region.

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19. (New) The semiconductor device as claimed in claim 17, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

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20. (New) The semiconductor device as claimed in claim 17, wherein the heavily doped region of the first conductivity type does not extend under a second MOS transistor in the second well.

21. (New) The semiconductor device as claimed in claim 15, further comprising a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well, wherein the heavily doped region of buried layer having a second conductivity type is formed between the first contact region in the first well and an interface between the first well and the semiconductor substrate.

22. (New) The semiconductor device as claimed in claim 21, further comprising:
a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and
a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between the second well and the semiconductor substrate.

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~~23. (New) The semiconductor device as claimed in claim 15, wherein the heavily doped region of the second conductivity type does not extend under a first MOS transistor in the first well.~~

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~~24. (New) A semiconductor device comprising:
a semiconductor substrate having a first conductivity type;
a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well;
a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;
a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well;
a heavily doped region of buried layer having the second conductivity type formed between the first contact region in the first well and an interface between the first well and the semiconductor substrate and not formed at an interface between the first and second wells; and
a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between the second well and the semiconductor substrate.~~

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Cmpl'd.* 25. (New) The semiconductor device as claimed in claim 22, wherein the heavily doped region of buried layer having a first conductivity type is not formed at an interface between the first and second wells.
